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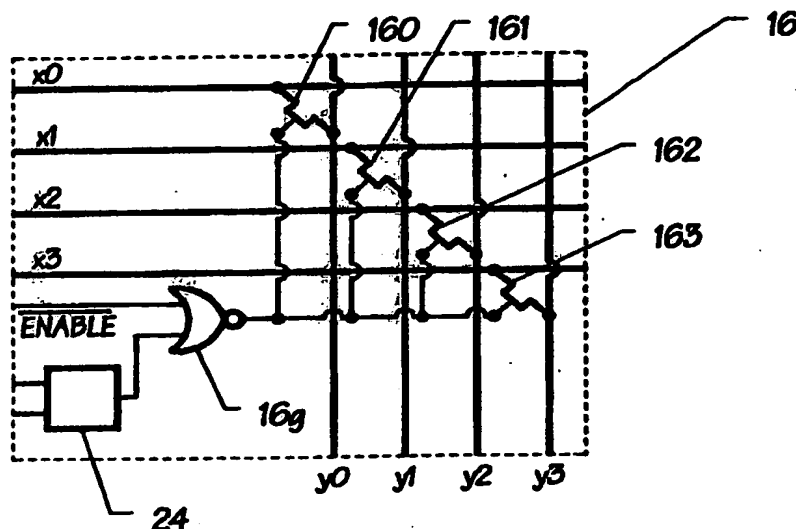
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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : H03K 19/177		A1	(11) International Publication Number: WO 98/33276
			(43) International Publication Date: 30 July 1998 (30.07.98)
(21) International Application Number: PCT/GB98/00248		(81) Designated States: JP, US, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).	
(22) International Filing Date: 28 January 1998 (28.01.98)		Published With international search report.	
(30) Priority Data: 97300562.2 29 January 1997 (29.01.97) EP (34) Countries for which the regional or international application was filed: GB et al.			
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(54) Title: FIELD PROGRAMMABLE PROCESSOR



(57) Abstract

A field programmable device comprises: an array of processing devices; a connection matrix interconnecting the processing devices and including switches (160-163); and memory cells (24) for storing data for controlling the switches to define the configuration of the interconnections of the connection matrix. In order to provide flexible use of memory and to enable higher memory densities, gates (16g, 18g, 20g) are provided which can be used to isolate the effect of the data stored in at least one group of the memory cells and switches on the configuration of the interconnections so that the memory cells in that group are available for storing other data.

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TITLE

FIELD PROGRAMMABLE PROCESSOR

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DESCRIPTION

This invention relates to a field programmable devices.

- 10 In particular, the invention relates to such a device comprising: a plurality of processing devices; a connection matrix interconnecting the processing devices and including a plurality of switches; a plurality of memory cells for storing data for controlling the switches to define the configuration of the interconnections of the connection matrix.
- 15 The problems with which the present invention (or at least preferred embodiments of it) is concerned are to provide more flexible use of memory, to enable higher memory density and higher circuit density.

- In accordance with a first aspect of the present invention, there is provided means for
- 20 isolating the effect of the data stored in at least one group of the memory cells and switches on the configuration of the interconnections so that the memory cells in that group are available for storing other data. Accordingly, the memory cells can be selectively used (a) for controlling the interconnections and (b) as user memory. By providing this feature using the configuration memory for the switches, higher memory
- 25 density can be achieved.

- In one embodiment, the isolating means comprises means for isolating each of the memory cells in the group from the switches. This enables isolation without requiring additional switches to be introduced into the wiring of the connection matrix, which
- 30 would increase signal propagation delay and so reduce circuit speed.

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adjacent the switch or switches controllable by that memory cell, thus enabling circuit density to be achieved.

This latter feature may be provided, whether or not the memory cells are is

5 Therefore, in accordance with a third aspect of the present invention, there is a field programmable device, comprising: a plurality of processing devices; a connection matrix interconnecting the processing devices and including a plurality of switches; a plurality of memory cells for storing data for controlling the switches to determine a configuration of the interconnections of the connection matrix; wherein the positions of the memory cells are distributed across the device to substantially the same extent as the switches, and each of the memory cells is disposed adjacent the switch or switches controllable by that memory cell.

14 A specific embodiment of the present invention will now be described, by example, with reference to the accompanying drawings, in which:

15 Figure 1 shows part of a processor array, illustrating six switching sections and the locations of six arithmetic logic units;

20 Figure 2 is a diagram of part of the arrangement shown in figure 1 on a large scale, illustrating one of the switching sections and one of the locations of the arithmetic logic units;

24 Figure 3 shows part of the processor array shown in figure 1 on a smaller scale, illustrating the locations of the arithmetic logic units and "vertical" busses extending across them;

30 Figure 4 is similar to figure 3, but illustrating "horizontal" busses extending across the locations of the arithmetic logic units;

Figure 5 shows the interconnections between the busses of figures 2, 3 and

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preferably square) array of "tiles" 10, one of which is shown bounded by a thick line in figure 1. Any appropriate number of tiles may be employed, for example in a 16 x 16, 32 x 32 or 64 x 64 array. Each tile 10 is rectangular (and preferably square) and is divided into four circuit areas. It is preferable for these tiles to be logically square (to provide symmetry in connection), although it is of less significance that they be physically square (this may have some advantage in providing symmetry in timing, but this will generally be less likely to be of significance). Two of the circuit areas 12, which are diagonally opposed in the tile 10, provide the locations for two arithmetic logic units ("ALUs"). The other two circuit areas, which are diagonally opposed in the tile 10, provide the locations for a pair of switching sections 14.

Referring to figures 1 and 2, each ALU has a first pair of 4-bit inputs a, which are directly connected within the ALU, a second pair of 4-bit inputs b, which are also directly connected within the ALU, and four 4-bit outputs f, which are directly connected within the ALU. Each ALU also has an independent pair of 1-bit carry inputs hci, vci, and a pair of 1-bit carry outputs co, which are directly connected within the ALU. The ALU can perform standard operations on the input signals a, b, hci, vci to produce the output signals f, co, such as add, subtract, AND, NAND, OR, NOR, XOR, NXOR and multiplexing and optionally can register the result of the operation. The instructions to the ALUs may be provided from respective 4-bit memory cells whose values can be set via the "H-tree" structure described below, or may be provided on the bus system which will be described below.

At the level shown in figures 1 and 2, each switching section 14 has eight busses extending across it horizontally, and eight busses extending across it vertically, thus forming an 8 x 8 rectangular array of 64 crossing points, which have been numbered in figure 2 with Cartesian co-ordinates. All of the busses have a width of four bits, with the exception of the carry bus vc at X=4 and the carry bus hc at Y=3, which have a width of one bit. At many of the crossing points, a 4-gang programmable switch 16 is provided which can selectively connect the two busses at that crossing point. At some of the crossing points, a 4-gang programmable switch 18 is provided which can

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selectively connect two busses which meet end to end at that crossing point, without any connection to the bus at right angles thereto. At the crossing point at (4, 3), a programmable switch 20 (for example as shown in Figure 6C) is provided which can selectively connect the carry busses vc, hc which cross at right angles at that point.

5

The horizontal busses in the switching section 14 will now be described.

At Y=0, busses h2s are connectable by programmable switches 16 to the vertical busses at X=0, 1, 2, 5, 6. The busses h2s have a length of two tiles and are connectable end to end in every other switching section 14 by a programmable switch 18 at (4, 0).

10

At Y=1, a bus be extending from an input b of the ALU to the West is connectable by switches 16 to the vertical busses at X=0, 1, 2, 3. Also, a bus fw extending from an output f of the ALU to the East is connectable by switches 16 to the vertical busses at X=5, 6, 7. The ends of the busses be, fw are connectable by a programmable switch 18 at (4, 1).

15

At Y=2, a bus hregs is connectable by programmable switches 16 to the vertical busses at X=1, 2, 3, 5, 6, 7.

20

At Y=3, a bus hco extends from the carry output co of the ALU to the West to a programmable switch 20 at (4, 3), which can connect the bus hco (a) to a carry bus hci extending to the carry input hci of the ALU to the East or (b) to a carry bus vci extending to the carry input vci of the ALU to the South.

25

At Y=4, a bus hregn is connectable by programmable switches 16 to the vertical busses at X=0, 1, 2, 3, 5, 6.

At Y=5, busses h1 are connectable to the vertical busses at X=0, 1, 2, 3, 5, 6, 7. The busses h1 have a length of one tile and are connectable end to end in each switching section 14 by a programmable switch 18 at (4, 5).

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At $Y=6$, a bus fe extending from an output f of the ALU to the West is connectable by switches 16 to the vertical busses at $X=0, 1, 2, 3$. Also, a bus aw extending from an input a of the ALU to the East is connectable by switches 16 to the vertical busses at $X=5, 6, 7$. The ends of the busses fe, aw are connectable by a programmable switch 18 at (4, 6).

At $Y=7$, busses $h2n$ are connectable by programmable switches 16 to the vertical busses at $X=1, 2, 3, 6, 7$. The busses $h2n$ have a length of two tiles and are connectable end to end in every other switching section 14 by a programmable switch 18 at (4, 7), staggered with respect to the programmable switches 18 connecting the busses $h2s$ at (4, 0).

The vertical busses in the switching section 14 will now be described.

At $X=0$, busses $v2w$ are connectable by programmable switches 16 to the horizontal busses at $Y=0, 1, 4, 5, 6$. The busses $v2w$ have a length of two tiles and are connectable end to end in every other switching section 14 by a programmable switch 18 at (0, 3).

At $X=1$, a bus fn extending from an output f of the ALU to the South is connectable by programmable switches 16 to the horizontal busses at $Y=0, 1, 2$. Also, a bus bs extending from an input b of the ALU to the North is connectable by switches 16 to the horizontal busses at $Y=4, 5, 6, 7$. The ends of the busses fn, bs are connectable by a programmable switch 18 at (1, 3).

25

At $X=2$, busses $v1$ are connectable to the horizontal busses at $Y=0, 1, 2, 4, 5, 6, 7$. The busses $v1$ have a length of one tile and are connectable end to end in each switching section 14 by a programmable switch 18 at (2, 3).

At $X=3$, a bus $vregw$ is connectable by programmable switches 16 to the horizontal busses at $Y=1, 2, 4, 5, 6, 7$.

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At X=4, a bus vco extends from the carry output co of the ALU to the North to the programmable switch 20 at (4, 3), which can connect the bus vco (a) to the carry bus hci extending to the carry input hci of the ALU to the East or (b) to the carry bus vci extending to the carry input vci of the ALU to the South.

5

At X=5, a bus vrege is connectable by programmable switches 16 to the horizontal busses at Y=0, 1, 2, 4, 5, 6.

At X=6, a bus an extending from an input a of the ALU to the South is connectable by switches 16 to the horizontal busses at Y=0, 1, 2. Also, a bus fs extending from an output f of the ALU to the North is connectable by programmable switches 16 to the horizontal busses at Y=4, 5, 6, 7. The ends of the busses an, fs are connectable by a programmable switch 18 at (6, 3).

At X=7, busses v2e are connectable by programmable switches 16 to the horizontal busses at Y=1, 2, 5, 6, 7. The busses v2e have a length of two tiles and are connectable end to end in every other switching section 14 by a programmable switch 18 at (7, 3) staggered with respect to the programmable switches 18 connecting the busses v2w at (0, 3).

20

As shown in figure 2, the busses bs, vco, fs are connected to input b, output co and output f, respectively, of the ALU to the North of the switching section 14. Also, the busses fe, hco, be are connected to the output f, output co and input b of the ALU, respectively, to the West of the switching section 14. Furthermore, the busses aw, hci, fw are connected to the input a, input ci and output f, respectively, of the ALU to the East of the switching section 14. Moreover, the busses fn, vci, an are connected to the output f, input ci and input a, respectively, of the ALU to the south of the switching section 14.

25

In addition to these connections, the busses vregw, vrege are connected via respective programmable switches 18 to 4-bit connection points ytsw, vtse, respectively, (shown

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by crosses in Figure 2) in the area 12 of the ALU to the North of the switching section 14. Also, the busses hregs, hregn are connected via respective programmable switches 18 to 4-bit connection points htse, htne, respectively, in the area 12 of the ALU to the West of the switching section 14. Furthermore, the busses hregs, hregn are connected via respective programmable switches 18 to 4-bit connection points htsw, htnw, respectively, in the area 12 of the ALU to the East of the switching section 14. Moreover, the busses vregw, vreg are connected via respective programmable switches 18 to 4-bit connection points vtnw, vtne, respectively, in the area 12 of the ALU to the south of the switching section 14. These connection points vtnw, vtne, htne, htse, vtsw, htsw, htnw will be described below in further detail with reference to figures 3 to 5.

Also, as shown in figure 2, the busses hregn, vreg, hregs, vregw have respective 4-bit connection points 22 (shown by small squares in figure 2) which will be described below in further detail with reference to figure 9.

Figure 3 shows one level of interconnections between the locations of the arithmetic logic units, which are illustrated by squares with rounded corners. A group of four 4-bit busses v8, v4w, v4e, v16 extend vertically across each column of ALU locations 12. The leftmost bus v8 in each group is in segments, each having a length generally of eight tiles. The leftmost but one bus v4w in each group is in segments, each having a length generally of four tiles. The rightmost but one bus v4e in each group is in segments, again each having a length generally of four tiles, but offset by two tiles from the leftmost but one bus v4w. The rightmost bus v16 in each group is in segments, each having a length generally of sixteen tiles. At the top edge of the array, which is at the top of figure 4, and at the bottom edge the lengths of the segments may be slightly greater than or shorter than specified above.

Referring to figures 3 and 5, where each group of four busses v8, v4w, v4e, v16 crosses each ALU location 12, four 4-bit tap connections are made at the connection points htnw, htsw, htse, htne. The ends of the bus segments take priority in being so connected

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over a connection to a bus segment which crosses the ALU location.

Similarly, as shown in figures 4 and 5, a group of four 4-bit busses h8, h4n, h4s, h16 extend horizontally across each row of ALU locations 12. The uppermost bus h8 in each group is in segments, each having a length generally of eight tiles. The uppermost but one bus h4n in each group is in segments, each having a length generally of four tiles. The lowermost but one bus h4s in each group is in segments, again each having a length generally of four tiles, but offset by two tiles from the uppermost but one bus h4n. The lowermost bus h16 in each group is in segments, each having a length generally of sixteen tiles. At the left hand edge of the array, which is at the left of figure 4, and at the right hand edge the lengths of the segments may be slightly greater than or shorter than specified above. Where each group of busses h8, h4n, h4s, h16 crosses each ALU location 12, a further four 4-bit tap connections are made at the connection points vtnw, vtsw, vtse, vtne. The ends of the bus segments take priority in being so connected over a connection to a bus segment which crosses the ALU location.

As shown in figure 5, the connection points htnw, htsw, htne, htse are connected via programmable switches to the busses hregw, hreg of the switching sections to the West and the East of the ALU location. Also, the connection points vtnw, vtne, vtsw, vtse are connected via programmable switches to the busses vregw, vreg of the switching sections to the North and the South of the ALU location.

The programmable connections 16 between pairs of 4-bit busses which cross at right angles will now be described with reference to figure 6A. The conductors of the horizontal busses are denoted as x0, x1, x2, x3, and the conductors of the vertical busses are denoted as y0, y1, y2, y3. Between each pair of conductors of the same bit significance, a respective transistor 160, 161, 162, 163 is provided. The gates of the transistors 160, 161, 162, 163 are connected in common to the output of a NOR gate 16g, which receives as its two inputs an inverted ENABLE signal from a single bit memory cell, which may be shared by a group of the switches, and the inverted content of a single bit memory cell 24. Accordingly, only when the ENABLE signal is high and

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the content of the memory cell 24 is high, the conductors x0, x1, x2, x3 are connected by the transistors 160, 161, 162, 163, respectively, to the conductors y0, y1, y2, y3, respectively.

- 5 The programmable connections 18 between pairs of 4-bit busses which meet each other end to end in line will now be described with reference to figure 6B. The conductors of one bus are denoted as x10, x11, x12, x13, and the conductors of the other bus are denoted as x20, x21, x22, x23. Between each pair of conductors of the same bit significance, a respective transistor 180, 181, 182, 183 is provided. The gates of the
- 10 transistors 180, 181, 182, 183 are connected in common to the output of a NOR gate 18g, which receives as its two inputs an inverted ENABLE signal from a single bit memory cell, which may be shared by a group of the switches, and the inverted content of a single bit memory cell 24. Accordingly, only when the ENABLE signal is high and the content of the memory cell 24 is high, the conductors x10, x11, x12, x13 are
- 15 connected by the transistors 180, 181, 182, 183, respectively, to the conductors x20, x21, x22, x23, respectively.

- The programmable connections 20 between the carry conductors hco, vco, hci, vci will now be described with reference to figure 6C. The horizontal carry output conductor hco
- 20 is connected to the horizontal carry input conductor hci and the vertical carry input conductor vci via transistors 20hh, 20hv, respectively. Furthermore, the vertical carry output conductor vco is connected to the vertical carry input conductor vci and the horizontal carry input conductor hci via transistors 20vv, 20vh, respectively. The gates of the transistors 20hh, 20vv are connected in common to the output of an inverter 20i,
- 25 and the gates of the transistors 20hv, 20vh and the input to the inverter 20i are connected to the output of a NOR gate 20g. The NOR gate 20g receives as its two inputs an inverted ENABLE signal from a single bit memory cell, which may be shared by a group of the switches, and the inverted content of a single bit memory cell 24. Accordingly, when the ENABLE signal is high, the conductors hco, vco are connected
- 30 to the conductors hci, vci, respectively, or to the conductors vci, hci, respectively, in dependence upon the content of the memory cell 24.

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It will be noted that each of the switchable connections 16, 18, 20 described with reference to figures 6A to 6C includes a NOR gate 16g, 18g, 20g. As shown in figure 7, a NOR gate 16g is typically formed by four transistors 16g1, 16g2, 16g3, 16g4, two 16g1, 16g3 of which are responsive to the inverted ENABLE signal, and two 16g2, 16g4 of which are responsive to the inverted content of the memory cell 24. In the embodiment of the invention, it is desirable that a group of the switchable collections 16, 18, 20 may be disabled in common, without any need for only part of such a group to be disabled. Such a group might consist of all of the switchable connections in one switching section 14, all of the switchable connections in the two switching sections 14 in a particular tile, or all of the switchable connections in a larger area of the array. In this case, the transistor 16g1 may be made common to all of the switchable connections 16, 18, 20 in the group, as shown in figure 8. This enables a 25% less one saving in the number of transistors required for the gates, but does require a further conductor linking the gate, as shown in figure 8.

The man skilled in the art will appreciate that the structures depicted in Figures 7 and 8 can be modified for optimisation. For example, the arrangement of Figures 7 and 8 would not fully exploit memory cells 24 designed to return both a stored value and a complement of that stored value. Use of the complement obtained from such cells 24 could be used to obviate any need for both the ENABLE and inverted ENABLE signals to be carried to all of the switchable connections in a group, as is the case in Figure 8.

As mentioned above with reference to figures 1 and 2, at each switching section 14, the busses hreg_n, hreg_s, vreg_w, vreg_e are connected by respective 4-bit connections 22 to a register or buffer circuit, and this circuit will now be described in more detail with reference to figure 9. The four connections 22 are each connected to respective inputs of a multiplexer 26. The multiplexer 26th selects one of the inputs as an output, which is supplied to a register or buffer 28. The output of the register or buffer 28 is supplied to four tri-state buffers 30_s, 30_w, 30_n, 30_e, which are connected back to the connections 22 to the busses hreg_s, vreg_w, hreg_n, vreg_e, respectively. In the case where a buffer 28 is used, the 4-bit signal on a selected one of the busses hreg_s, vreg_w, hreg_n, vreg_e is

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amplified and supplied to another selected one of the busses hregs, vregw, hregw, vreg. In the case where a register 28 is used, the 4-bit signal on a selected one of the busses hregs, vregw, hregw, vreg is amplified and supplied to any selected one of the busses hregs, vregw, hregw, vreg after the next active clock edge.

5

It will be appreciated that the arrangement described above provides great flexibility in the routing of signals around and across the array. With appropriate setting of the switches 16, 18, 20 using the memory cells 24 and with appropriate setting of the multiplexers 26 and registers or buffers 28, signals can be sent over large distances, primarily using the busses v16, h16, v8, h8, v4e, v4w, h4n, h4s from the edge of the array to a particular ALU, between ALUs, and from a particular ALU to the edge of the array. These busses can be joined together in line, or at right angles, by the switching sections 14, with amplification by the registers or buffers 28 in order to reduce propagation delays, and with pipeline stages introduced by the registers 28. Also, these busses can be tapped part way along their lengths, so that the siting of the ALUs to perform a particular processing operation is not completely dictated by the lengths of the busses, and so that signals can be distributed to more than one ALU. Furthermore, the shorter length busses described with reference to figures 1 and 2 can be used to route signals between the switching sections 14 and the ALUs, and to send signals primarily over shorter distances, for example from one ALU to an adjacent ALU in the same row or column, or diagonally adjacent, even though the busses extend horizontally or vertically. Again, the registers or buffers 28 can be used to amplify the signals or introduce programmable delays into them.

25 In the arrangement described above, the memory cells 24 are distributed across the array to the same extent as the switching sections 14 and the ALU locations 12. Each memory cell 24 is disposed adjacent the switch or switches, multiplexer, register or buffer which it controls. This enables a high circuit density be achieved.

30 A description will now be made of the manner in which data is written to or read from the memory cells 24, the way in which the ENABLE signals for the programmable

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switches 16, 18, 20 are written to their memory cells, the way in which instructions, and possibly constants, are distributed to the ALUs, and the way in which other control signals, such as a clock signal, are transmitted across the array. For all of these functions, an "H-tree" structure (which is known per se) may be employed, as shown
5 in figure 10. Referring to Figures 10 and 11, in order to distribute an ENABLE signal to any of 64 locations in the example shown, the ENABLE signal 30a and a 6-bit address 32a for it are supplied to a decoder 34a. The decoder 34a determines which of the four branches from it leads to the address and supplies an ENABLE signal 30b to a further decoder 34b in that branch, together with a 4-bit address 32b to the decoders 34b
10 in all four branches. The decoder 34b receiving the ENABLE signal 30b determines which of the four branches from it leads to the required address and supplies an ENABLE signal 30c to a further decoder 34c in that branch, together with a 4-bit address 32c to the decoders 34c in all four branches. The decoder 34c receiving the ENABLE signal 30c then supplies the ENABLE signal 34d to the required address
15 where it can be stored in a single bit memory cell. An advantage of the H-tree structure is that the lengths of the signal paths to all of the destinations are approximately equal, which is particularly advantageous in the case of the clock signal.

A great advantage of the arrangement described above is that groups of the memory cells
20 24 in for example one switching section 14, or in the two switching sections in one tile, or in the switching sections in a sub-array of the tiles may be disabled en bloc by the inverted ENABLE signals so that the contents of those memory cells do not affect the associated switches. It is then possible for those memory cells 24 to be used as "user" memory by an application, rather than being used for configuring the wiring of the
25 array.

The embodiment of the invention has been described merely by way of example, and many modifications and developments may be made in keeping with the present invention. For example, the embodiment employs ALUs as the processing units, but
30 other processing units may additionally or alternatively be used, for example look-up tables, programmable logic arrays and/or self-contained CPUs which are able to fetch

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their own instructions.

Furthermore, the embodiment has been described as if the whole array is covered by ALUs and switching sections. However, other types of section may be included in the array. For example, a sub-array might be composed of a 4 x 4 arrangement of tiles of ALUs and switching sections as described above, and the array might be composed of such sub-arrays and memory in a 4 x 4 array, or such sub-arrays and RISC CPUs in a 4 x 4 array.

10 In the embodiment described above, each ALU location is square, and each switching section is square and of the same size as the ALU locations, but it should be noted that the controllable switches 18 in the register busses vregw, vregc, hregw, hregc encroach into the square outline of the ALU locations. The ALU locations need not be of the same size as the switching sections, and in particular may be smaller, thus permitting one or more busses to pass horizontally or vertically directly from one switching section 14 to a diagonally adjacent switching section 14, for example running between the busses h2s, h2n or between the busses v2e, v2w.

In the embodiment described above, each ALU has two independent carry inputs vci, hci and a connected pair of carry outputs co. If required, the ALUs may be arranged to deal with two types of carry: a fast carry between adjacent ALUs which may be of particular use for multi-bit adding operations; and a slow carry which can be routed more flexibly and may be of particular use for digital serial arithmetic. The fast carry might be arranged in a similar manner to that described above with reference to the drawings, whereas the slow carry might employ programmable switches in the switching sections 14 between the carry conductor and particular bits of the 4-bit busses.

In the embodiment described above, particular bit widths, sizes of switching section and sizes of array have been mentioned, but it should be noted that all of these values may be changed as appropriate. Also, the programmable switches 16, 18, 20 have been described as being disposed at particular locations in each switching section 14, but other

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locations may be used as required and desired.

5 In the embodiment described above, the array is two-dimensional, but the principles of the invention are also applicable to three-dimensional arrays, for example by providing a stack of the arrays described above, with the switching sections in adjacent layers staggered with respect to each other. The stack might include just two layers, but preferably at least three layers, and the number of layers is preferably a power of two.

10 In the embodiment described above, the memory cells 24 can be isolated by the gates 16g, 18g, 20g from the switches which they control so that the memory cells can be used for other purposes, that is put in the "user plane". The ENABLE signal memory cells, however, cannot be transferred to the user plane. In an alternative embodiment, the switches in a particular switching section 14 may be disconnectable from the remainder of the array by further switches in the busses at the boundary of that switching section
15 14, with the further switches being controlled by a further memory cell which cannot be transferred to the user plane.

Many other modifications and developments may also be made.

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CLAIMS

1. A field programmable device, comprising:
a plurality of processing devices;
5 a connection matrix (14) interconnecting the processing devices and including a plurality of switches (16, 18, 20);
a plurality of memory cells (24) for storing data for controlling the switches to define the configuration of the interconnections of the connection matrix; and
means (16g, 18g, 20g) for isolating the effect of the data stored in at least one
10 group of the memory cells and switches on the configuration of the interconnections so that the memory cells in that group are available for storing other data.
2. A device as claimed in claim 1, wherein the isolating means comprises means (16g, 18g, 20g) for isolating each of the memory cells in the group from the switches:
15
3. A field programmable device, comprising:
a plurality of processing devices;
a connection matrix (14) interconnecting the processing devices and including a plurality of switches (16, 18, 20);
20 a plurality of memory cells (24) for storing data for controlling the switches to define the configuration of the interconnections of the connection matrix; and
means (16g, 18g, 20g) for isolating each of the memory cells from the switch or switches controllable by that memory cell.
- 25 4. A device as claimed in claim 2 or 3, wherein the isolating means is operable to set each of the switches in the group to a predetermined state upon isolation from the respective memory cell.
5. A device as claimed in any of claims 2 to 4, wherein the isolating means
30 comprises, for each memory cell, a respective gate (16g, 18g, 20g) having inputs connected to the memory cell and to a control signal (ENABLE), and having an output

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connected to the or each switch which can be controlled by that memory cell.

6. A device as claimed in claim 5, wherein each gate is provided by four transistors (16g1-16g4).

5

7. A device as claimed in claim 6, wherein one of the transistors (16g1) of each gate is common to a plurality of the gates.

8. A device as claimed in claim 1, wherein the isolating means comprises means for isolating each of the switches in the group from the remainder of the connection matrix.

10

9. A device as claimed in any preceding claim, wherein at least some of the interconnections provided by the connection matrix are in the form of plural-bit busses; and those of the switches for the busses each comprise a plurality of switch elements (160-163, 180-183) each for a respective bit of the bus.

15

10. A device as claimed in any preceding claim, wherein the positions of the memory cells are distributed across the device to substantially the same extent as the switches, and each of the memory cells is disposed adjacent the switch or switches controllable by that memory cell.

20

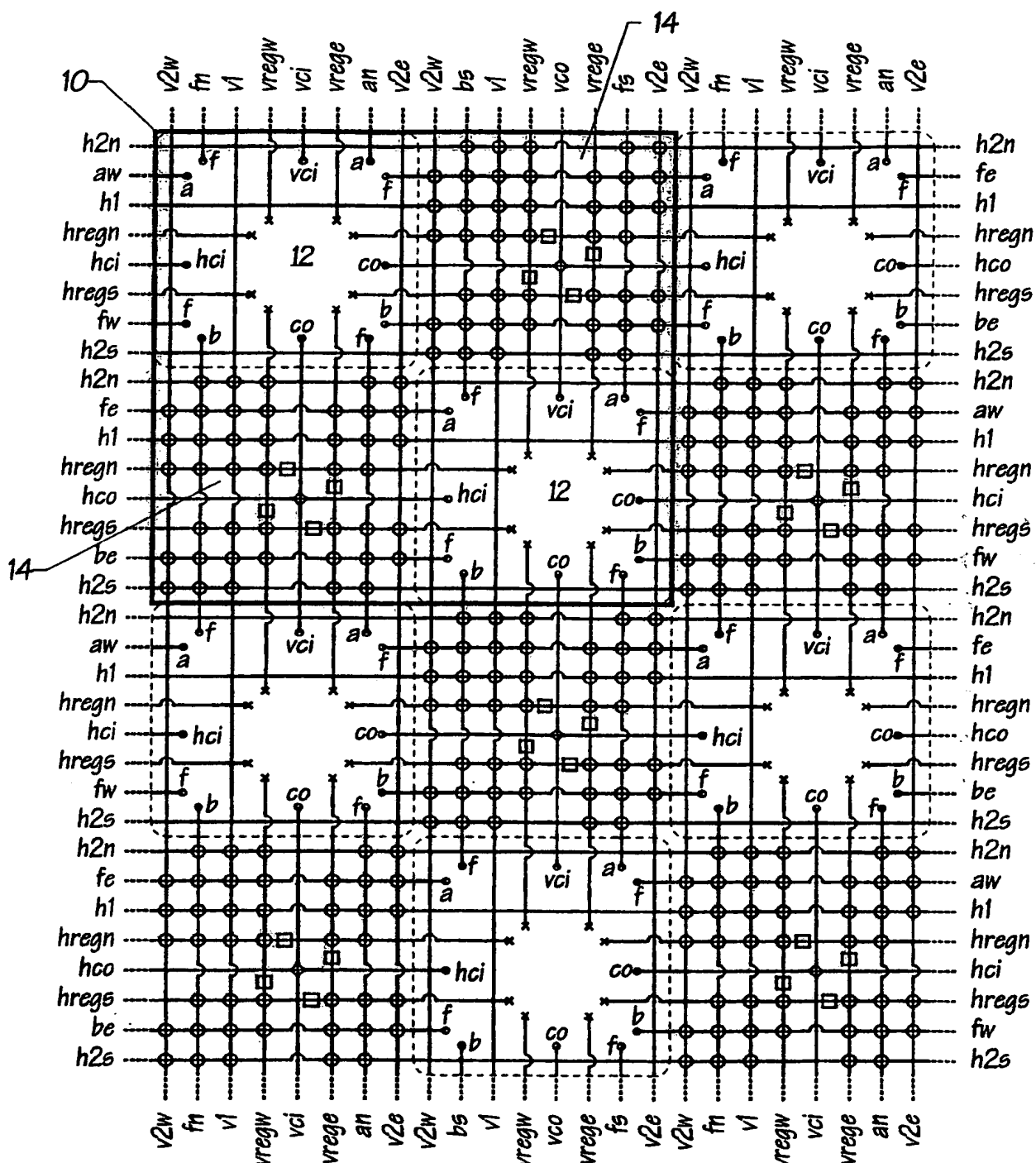


FIG. 1

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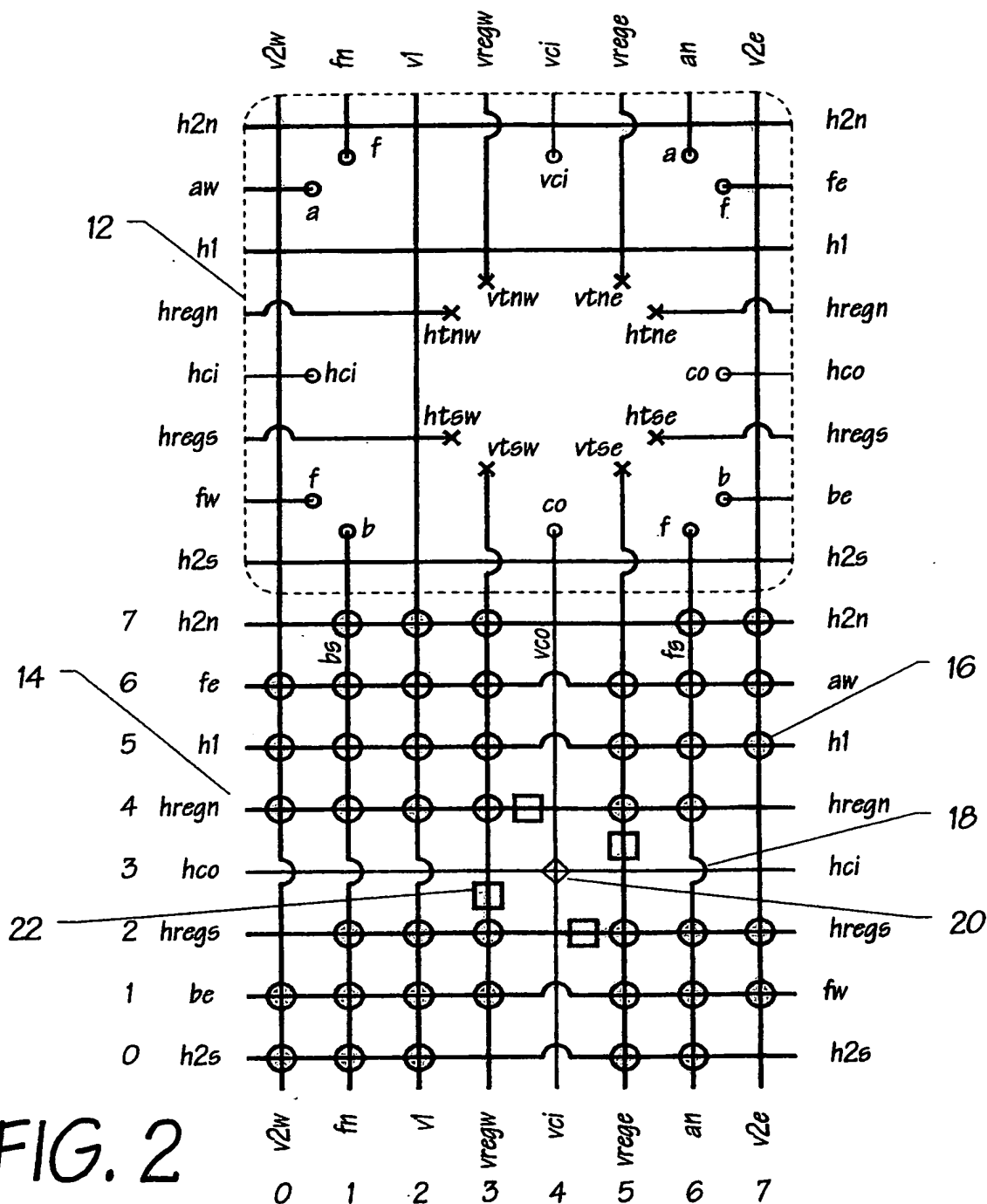
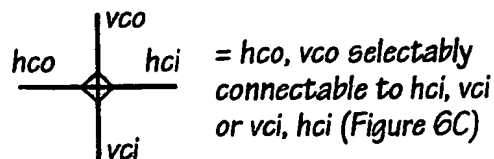
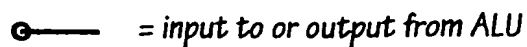
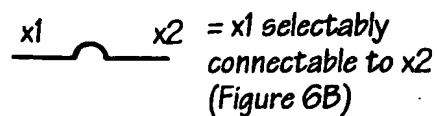
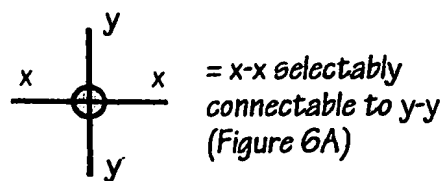


FIG. 2



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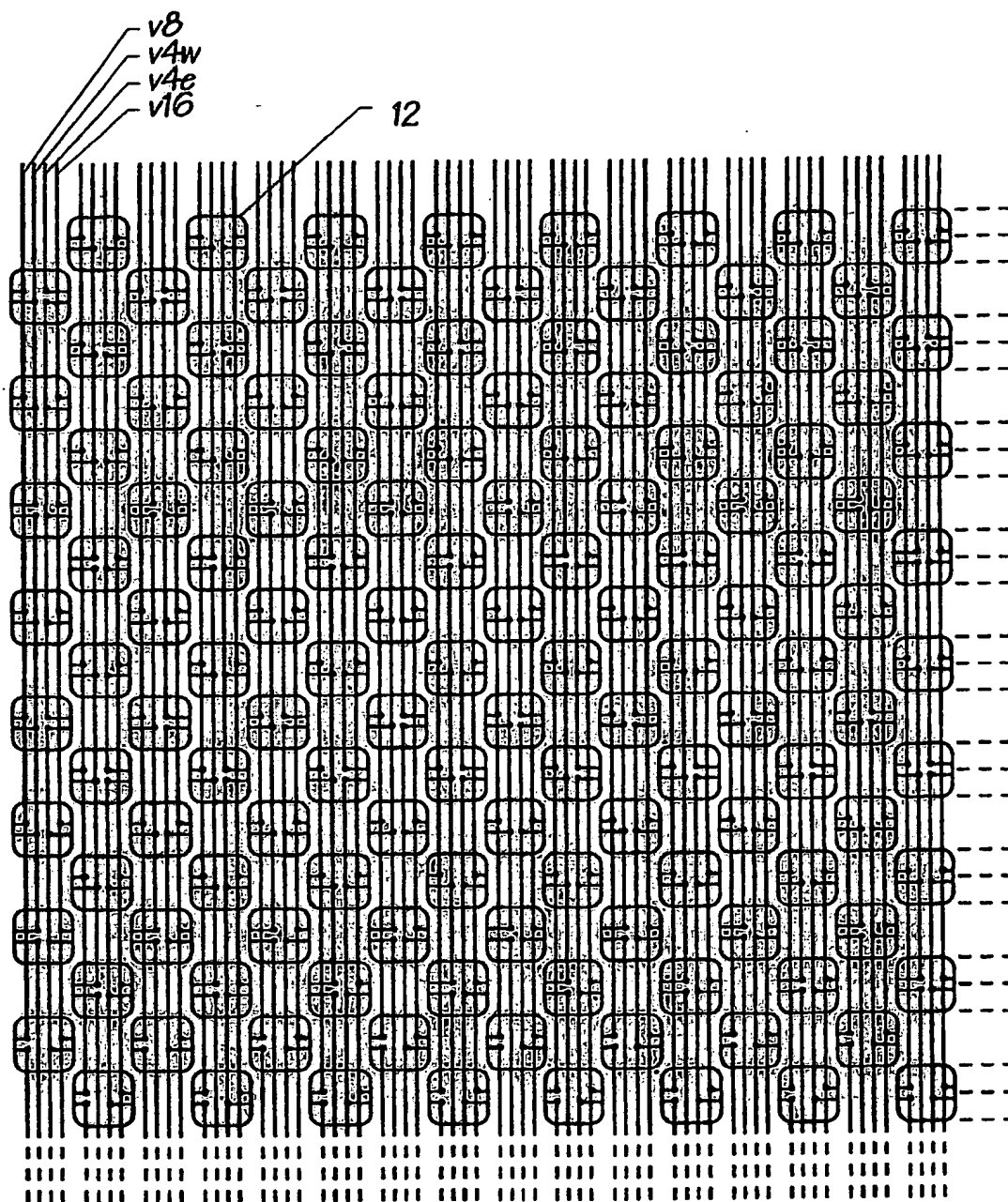


FIG. 3

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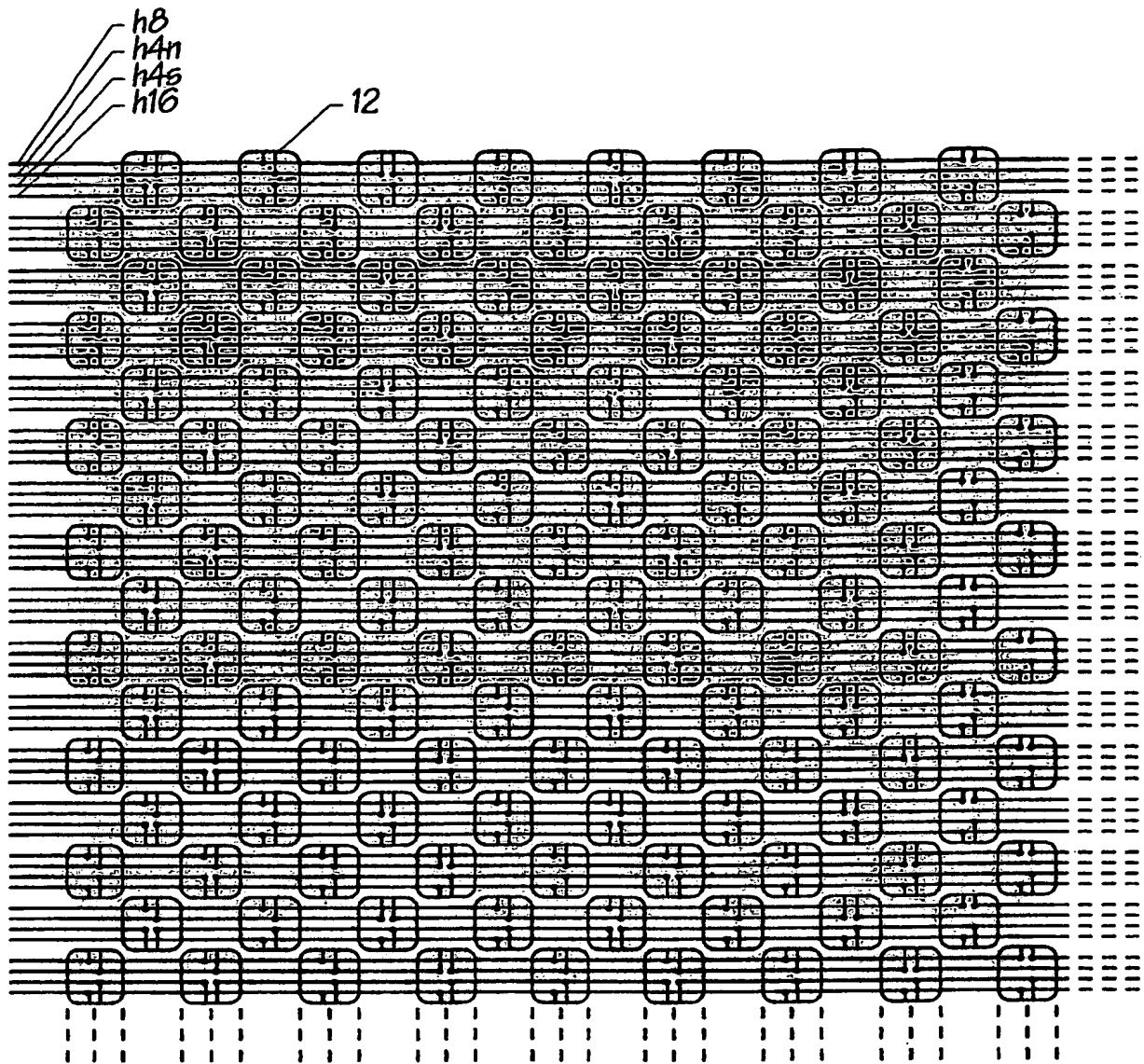


FIG. 4

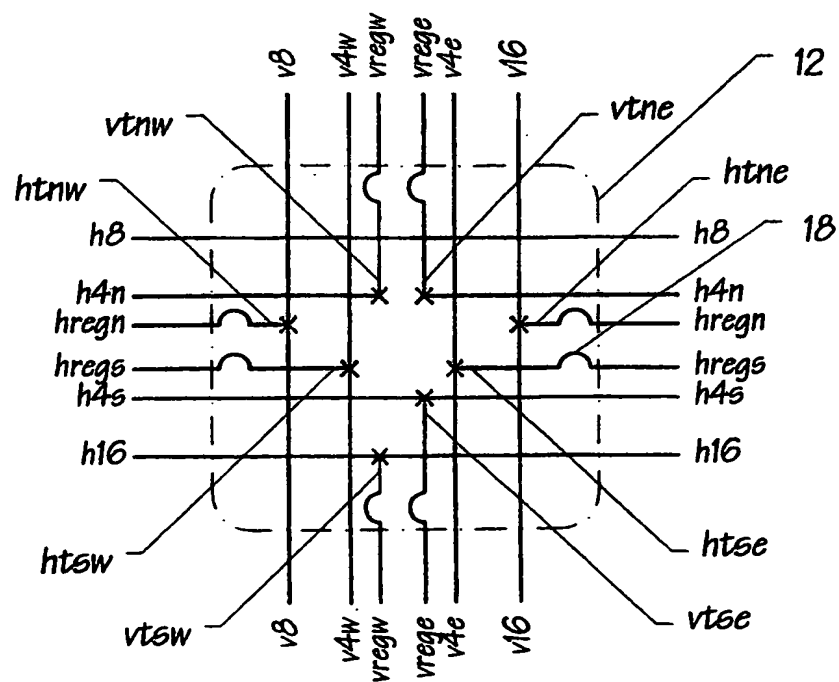


FIG. 5

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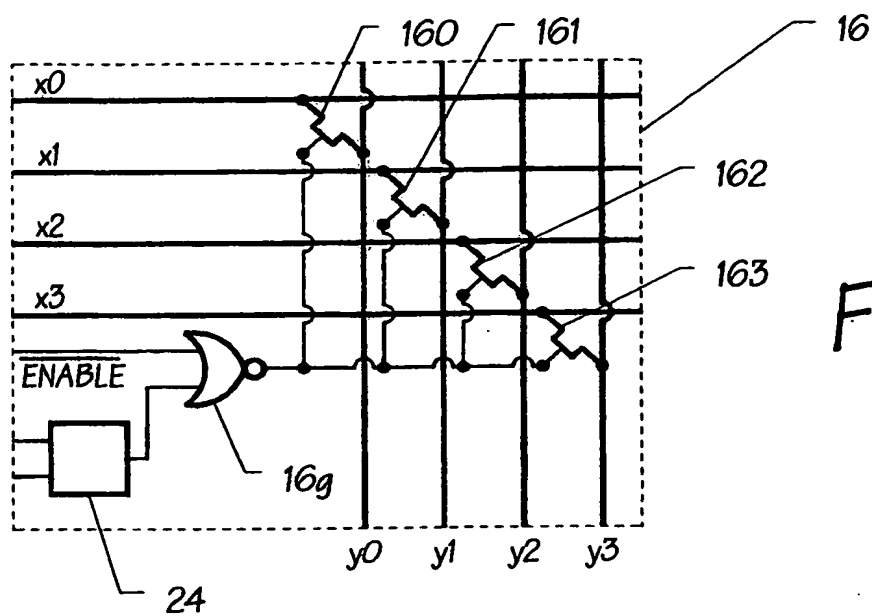
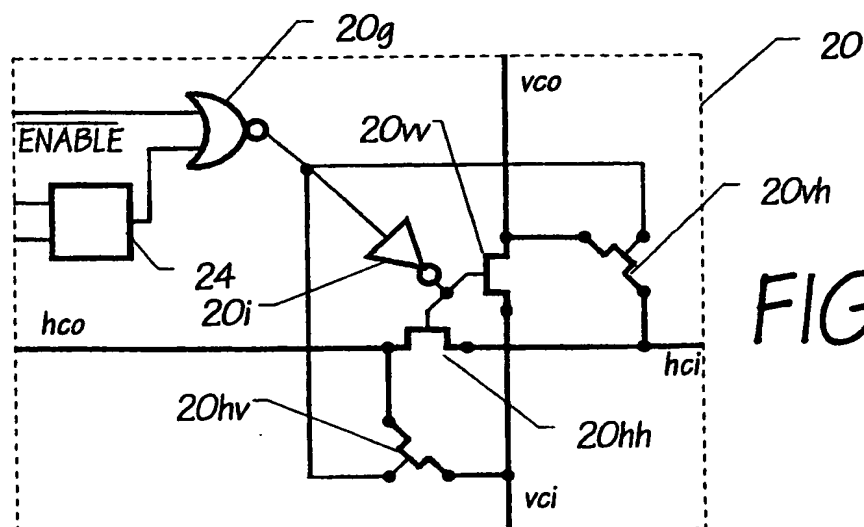
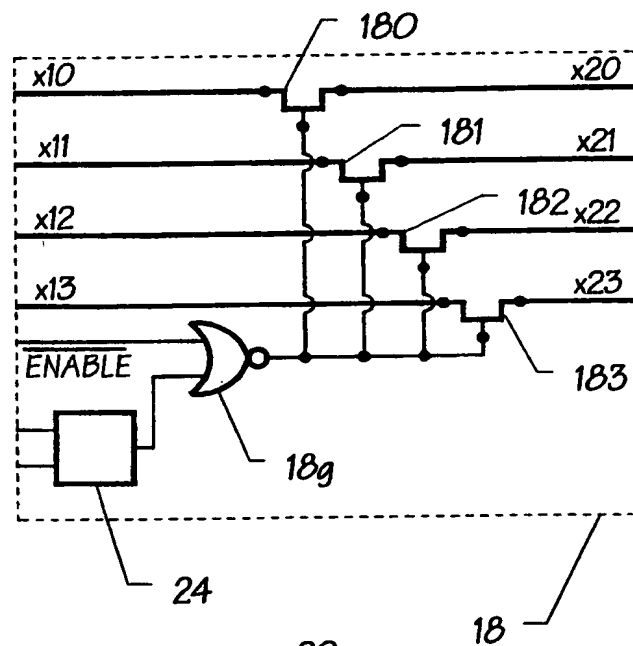


FIG. 6B



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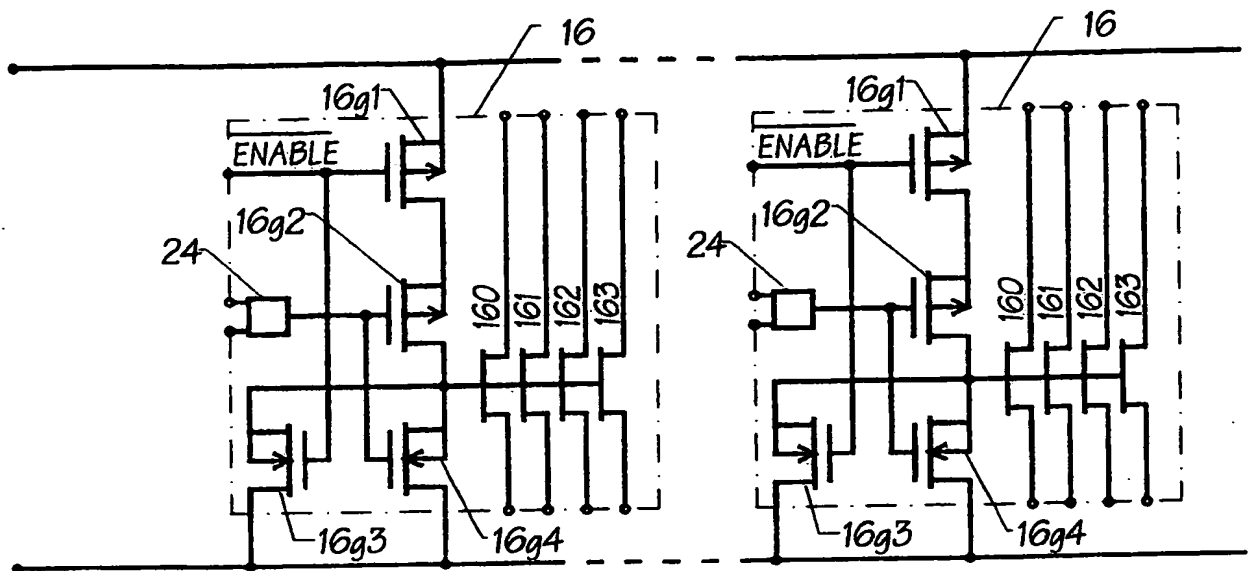


FIG. 7

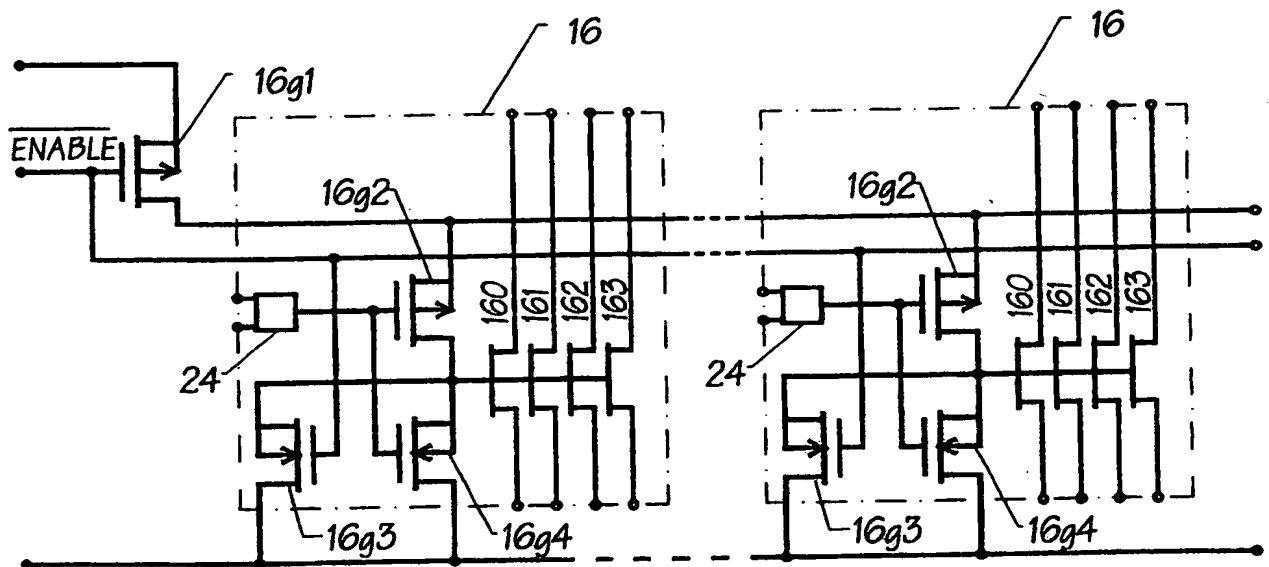


FIG. 8

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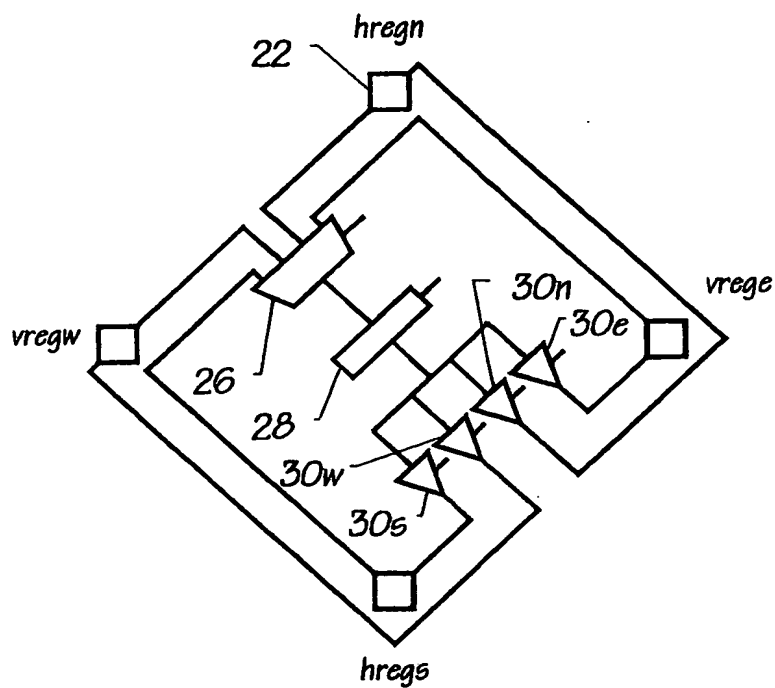


FIG. 9

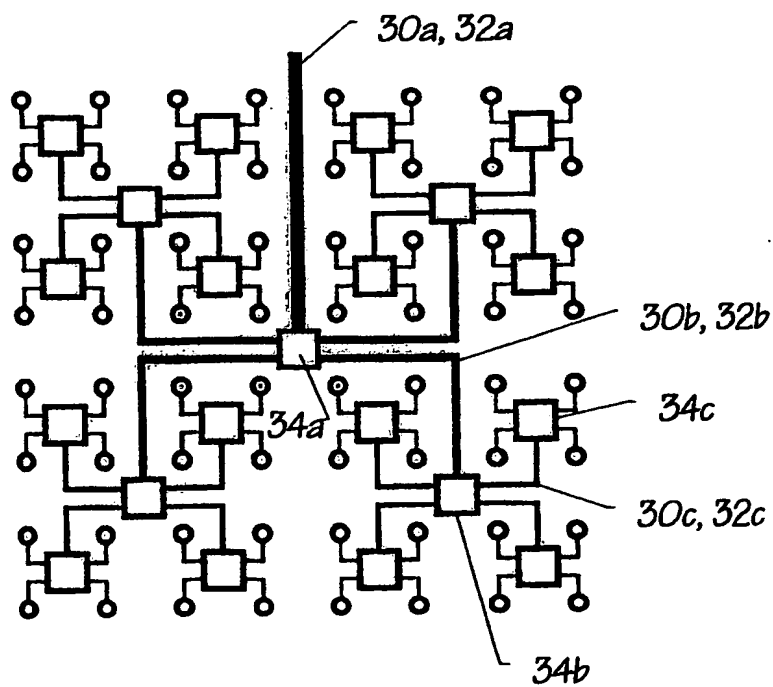


FIG. 10

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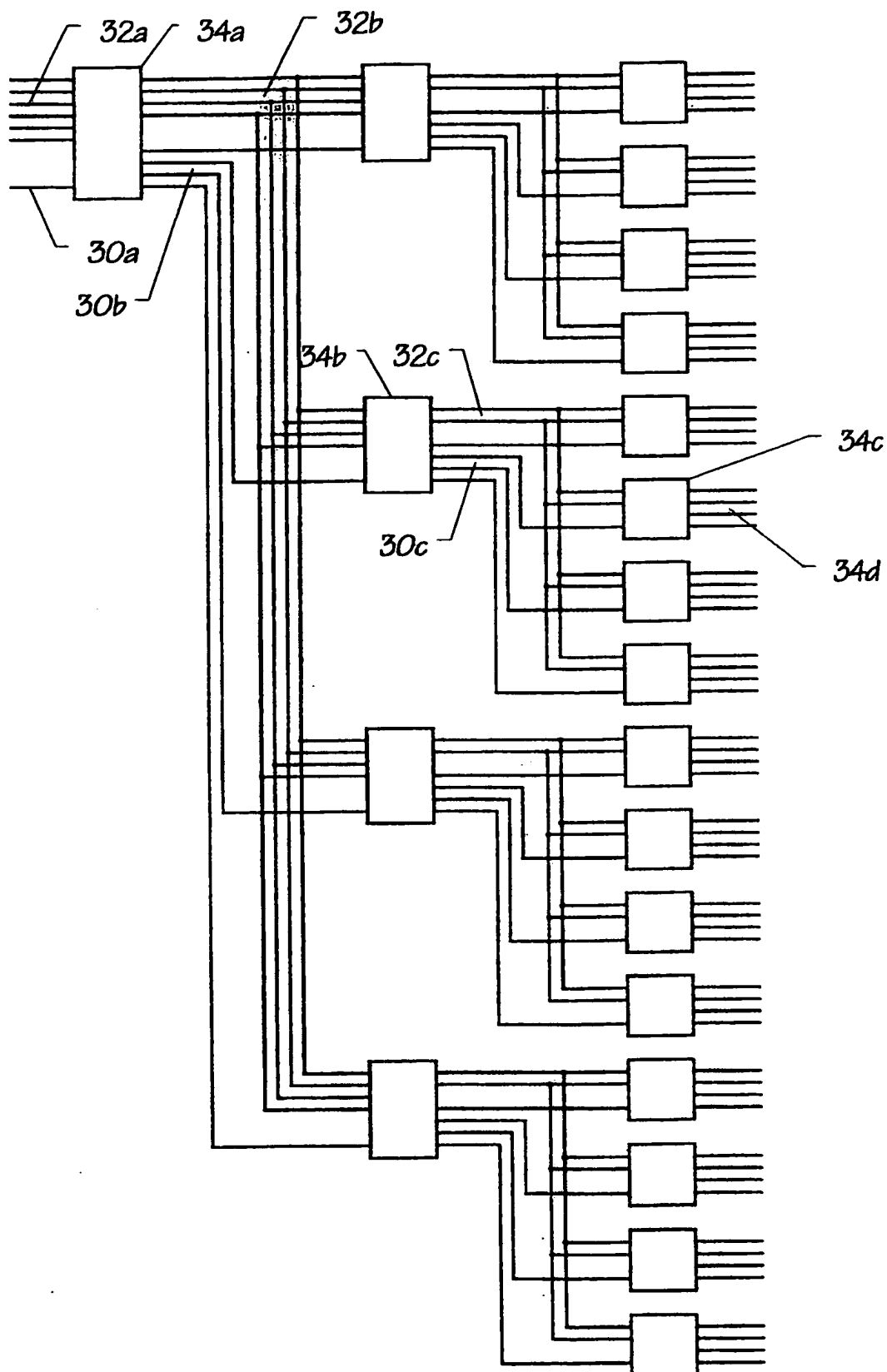


FIG. 11

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INTERNATIONAL SEARCH REPORT

Interr. Appl. No.

PCT/GB 98/00248

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H03K19/177

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H03K G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 583 450 A (TRIMBERGER STEPHEN M ET AL) 10 December 1996 see column 12, line 32 - column 13, line 64 ---	1-10
A	US 5 426 379 A (TRIMBERGER STEPHEN M) 20 June 1995 see column 3, line 35 - column 5, line 45 ---	1,3
A	BURSKY D: "GATE ARRAYS FACE ONSLAUGHT OF DENSE AND FLEXIBLE FPGAS" ELECTRONIC DESIGN, vol. 43, no. 13, 26 June 1995, page 85/86, 88, 90, 94, 96 XP000531702 see page 86, right-hand column, line 16 - page 90, left-hand column, line 9 --- -/--	1-10



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

* Special categories of cited documents:

- "A" document defining the general state of the art which is not considered to be of particular relevance
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- "O" document referring to an oral disclosure, use, exhibition or other means
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- "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- "&" document member of the same patent family

Date of the actual completion of the international search

6 May 1998

Date of mailing of the international search report

15/05/1998

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INTERNATIONAL SEARCH REPORT

Intern. Appl. No.

PCT/GB 98/00248

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>D. BURSKY: "SRAM BLOCKS AND ANTIFUSE LOGIC COMBINE IN NEW FPGAS" ELECTRONIC DESIGN, vol. 43, no. 16, 7 August 1995, CLEVELAND, USA, page 115, 116, 118 XP000531682 see page 118, middle column, line 12 - line 16</p>	1,3
A	<p>-----</p> <p>BORRIELLO G ET AL: "THE TRIPTYCH FPGA ARCHITECTURE" IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, vol. 3, no. 4, 1 December 1995, pages 491-500, XP000542422 see the whole document</p> <p>-----</p>	1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/GB 98/00248

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5583450 A	10-12-96	NONE	
US 5426379 A	20-06-95	NONE	

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